SYSTEM AND METHOD FOR SEQUENCING
MULTIPLE WRITE STATE MACHINES

BACKGROUND

[0001]   The size of electronic systems is constantly being reduced. For electronic systems that require memory devices, one way to reduce the size of the overall system is to use multiple memory arrays, which are typically stacked vertically on top of one another to minimize package area on the circuit board. Multi chip packages of flash memory are especially beneficial for compact devices, such as cellular telephones, personal digital assistants (PDAs), computers, electronic books, handheld electronic games, and the like. However, in many multi chip packages, the cost associated with the memory arrays increases to accommodate the larger amounts of aggregated current required to program each array of the multi chip package simultaneously.

[0002]   For example, in an electronic system having stacked flash memory, each flash memory typically has a controller, or a write state machine ("WSM"), that performs the flash erase and program operations. Each WSM follows a precise algorithm to program the individual flash memory. Associated with the algorithm is a current draw waveform associated with the current draw. A typical current draw waveform includes a large initial current pulse, which places a voltage on the memory cell, followed by a long pause, in which the WSM determines that the memory cell is responding to the input and a series of smaller pulses, which are used to build the voltage across the memory cell to a predetermined level for an appropriate state. To prevent a voltage overload to the system, the system must incorporate a voltage regulator that is capable of accommodating at least the maximum peak of the current draw profile and that ensures that the correct voltage on the array is maintained.

[0003]   In current systems, the voltage regulator is just large enough to accommodate a little more current than what is at the maximum peak of the current waveform. Many voltage regulators in current systems are not capable of sustaining any larger amounts of current, as larger voltage regulators tend to be more expensive.

[0004]   A problem arises when a stacked memory array is placed in an existing system with a voltage regulator capable of accommodating only a certain amount of voltage. Presently, the current waveform from each WSM is applied to each memory array in the stack simultaneously. Therefore, in order to program multiple memory arrays within the stack, the amplitude of the current waveform must be multiplied by the number of memory arrays within a given stack. For example, if two memory arrays are stacked and are to be programmed simultaneously, then the maximum current needed to program the two arrays must be twice the amount of current required to program one memory array. Because many systems have voltage regulators that are just large enough to accommodate a little more than the maximum peak of the current waveform for a single memory array, a new voltage regulator capable of accommodating a larger voltage must be installed in the system.

[0005]   Unfortunately, increasing the amount of current required to simultaneously program multiple stacked memory arrays requires larger voltage regulators and increases system costs. One way to avoid the costs of simultaneously programming multiple stacked memory arrays is to program the arrays in sequence. For example, in a stacked memory array having two memory arrays, the first memory array would be programmed first, then the second memory array would be programmed. However, as each memory array usually takes several milliseconds to program, two memory arrays would require twice the amount of time needed to program a

single memory array, which slows down the overall speed of the systems and increases the system costs.

BRIEF DESCRIPTION OF THE FIGURES

[0006]   FIG. 1 illustrates a block diagram representation of a system that is configured to sequence multiple write state machines in accordance with some embodiments of the present invention.

[0007]   FIG. 2 illustrates a prior art waveform including a plurality of pulses of current that may be applied to a write state machine.

[0008]   FIG. 3 is a logical flow diagram illustrating a routine of sequencing multiple write state machines according to some embodiments of the present invention.

[0009]   FIG. 4 is a timing diagram illustrating a pair of current waveforms for programming a stacked memory array in accordance with one embodiment of the present invention.

[0010]   FIG. 5 is a timing diagram illustrating a pair of current waveforms for programming a stacked memory array in accordance with another embodiment of the present invention.

[0011]   FIG. 6 is a timing diagram illustrating a pair of current waveforms for programming a stacked memory array in accordance with still another embodiment of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0012]   Referring now to the drawings, in which like numerals represent like elements or steps throughout the several views, FIG. 1 illustrates a block diagram representation of a system 100 that may contain a processor 105, a memory controller 110, and a stacked memory array 115, which may contain a first memory array 120A and a second memory array 120B. The memory controller 110 may act as an interface to control the flow of data between the processor 105 and the stacked memory array 115. The controller 110 may be configured to sequence two write state machines 125A and 125B and to program the stacked memory array 115 having the first memory array 120A and the second memory array 120B in accordance with some embodiments of the present invention.

[0013]   Memory array 120A and memory array 120B may typically comprise arrays of memory cells. In an exemplary embodiment, the first memory array 120A and the second memory array 120B may be stacked vertically such that the second memory array 120B may be physically on top of the first memory array 120A. In an exemplary embodiment, the memory arrays 120 may typically be NOR flash memory arrays; however, those skilled in the art will appreciate that other types of memory arrays, including but not limited to, NAND flash memory, random access memory ("RAM"), static random access memory ("SRAM"), and the like may be used without deviating from the scope of the embodiments of the present invention. Although the stacked memory array 115 may be described in terms of two memory arrays, those skilled in the art will appreciate that the number of memory arrays 120 is not limited and may contain any number of individual memory arrays 120 without departing from the scope of the embodiments of the present invention.

[0014]   The write state machines **125A**, **125B** may be the internal controllers of the individual memory arrays **110A**, **110B**, respectively. The write state machines **125** may be operable to follow an algorithm to program the individual memory **120** by using pulses of current from a pulse generator **130**.

[0015]   The memory controller **110** may also include a pulse generator **130** that may be operable to generate a waveform containing a series of current pulses, which may be supplied to the write state machines **125**. The pulse generator **130** may also communicate with a delay circuit **135** that may be operable to inject a time delay between a first pulse of current applied to the first write state machine **125A** and a second pulse of current applied to the second write state machine **125B**.

[0016]   FIG. 2 illustrates a prior art waveform **200** including a plurality of pulses of current that may be generated by the pulse generator **130** and applied to the write state machines **125**. The waveform **200** may begin, in time, with a short initial pulse **205** of current having a large amplitude, which may typically be used to initiate a write or erase operation to the individual memory cell and also to supply the majority of the current to the cell of the memory **120**. In an exemplary embodiment, the initial pulse **205** may have an amplitude of 25.4 milliamperes for approximately 1 microsecond, and may have a pulse width of approximately 2 microseconds.

[0017]   After the initial pulse **205**, there may be a period of time, or a delay **210**, during which time the system **100** may read what current is on each cell of the memory array **120A**. In an exemplary embodiment, the delay **210** may be approximately 7 microseconds long at 3 milliamperes. After the delay **210**, there may be a second pulse **215**, which may be used to

supply additional current to the write state machine **105**. Unlike the initial pulse **205**, this second pulse **215** may have a peak amplitude that is less than the pulse amplitude of the initial pulse **205**. In an exemplary embodiment, the peak amplitude may have a plateau at 10.6 milliamperes and a pulse width of approximately 30 microseconds, with a rise time of approximately 2 microseconds. After this second pulse **215**, there may be a plurality of additional brief delays **220** with smaller pulses **225** therebetween. In an exemplary embodiment, the plurality of brief delays **220** with smaller pulses **225** therebetween may include three brief delays **220** and three pulses **225**. During the brief delays **220** the system **100** may read the voltage on the individual cells of the memory array **120A**. Each brief delay **220** may last for approximately 2 microseconds at about 4 milliamperes. The three pulses **225** may indicate when additional current is being supplied to the write state machine **125**. Each of the three pulses **225** may last for approximately 22 microseconds at 10.6 milliamperes.

[0018]   After the plurality of additional brief delays **220** and pulses **225**, there may be a second delay **230**, which may permit the system **100** to verify if there is enough voltage on each cell of the memory array **120A**. The second delay **230**, in an exemplary embodiment, may last for about 20 microseconds at 2 milliamperes. If the memory controller **110** determines that enough voltage has not been built up within the memory cell, then an additional plurality of pulses **225**, which are shown in the dashed line in the figure, may be generated by the pulse generator **130** to increase the voltage on the cells of the memory array **120A** to the appropriate value.

[0019]   Although an exemplary prior art waveform **200** having a plurality of pulses therein has been described as having certain properties, including amplitudes and durations of individual pulses, those skilled in the art will appreciate that pulses of current having other

amplitudes and durations, may be applied individually or in combination to the write state machines **125**, which may create other waveforms that are within the scope of the embodiments of the present invention. For example, another waveform within the scope of the embodiments of the present invention may have a series of pulses therein, wherein all pulses may be of equal amplitude, duration, and period, such as the waveforms depicted in FIG. 6.

[0020]   FIG. 3 is a logical flow diagram illustrating a routine **300** of sequencing multiple write state machines **125** according to some embodiments of the present invention. Starting at **310**, the pulse generator **130** may apply current, in the form of the first initial pulse **205A**, to the first write state machine **125A**. At **320**, the delay circuit **135** may inject a time-delay Δt into the system **100** so that the initial pulse **205B** applied to the second write state machine **125B** may occur during the time of the delay **210A** of the first write state machine **125A** in accordance with an exemplary embodiment of the present invention.

[0021]   In a second exemplary embodiment, at **320**, the delay circuit **135** may inject a time-delay Δt into the system **100** so that the initial pulse **205B** applied to the second write state machine **125B** may occur during the time of the delay **230A** between the first plurality of three brief delays **220A** and pulses **225A** and the second plurality of brief delays **220A** and pulses **225A** applied to the first write state machine **125A**. By applying the initial pulse **205B** during either the delay **210A** or the delay **230A**, the peaks of the initial pulses **205A** and **205B** may not align in time, thereby allowing the system **100** to accommodate all current without incorporating a larger voltage regulator.

[0022]   Then at **330**, the pulse generator **130** may apply current to the next write state machine **105**, which in an exemplary embodiment may be the second write state machine **105B**.

In an exemplary embodiment, the amount of time-delay Δt may be at least as long as the amount of time of the initial pulse **205** of the first waveform **200A** so as to prevent the initial pulses **205**, in the form of the waveform **200**, generated by the pulse generator **130** from occurring simultaneously or during the rise and fall interval of the first initial pulse **205** applied to the first write state machine **105A**. Thus, in an exemplary embodiment, the second waveform may be offset from the first waveform by at least 2 microseconds. This may assure that the initial pulses **205** of the first waveform **200A** and the second waveform **200B** do not line up, thereby minimizing the amount of current needed to generate waveforms **200** to the first and second memory arrays **120A**, **120B**.

[0023]   Although the routine **300** has been described with respect to two write state machines **125**, those skilled in the art will appreciate that the routine **300** may be applied to any number of write state machines **125**, such that there may be a time-delay Δt between subsequent pulses of current applied to subsequent write state machines **125**.

[0024]   FIG. 4 is a timing diagram illustrating a pair of current waveforms **200A**, **200B** for programming a stacked memory array **115** in accordance with one embodiment of the present invention. In an exemplary embodiment, the pulse generator **130** may apply the first pulse **205A** of current of the plurality of pulses, which together may form the first waveform **200A**, to the first write state machine **125A**. Then, the delay circuit **135** may inject a time-delay Δt before the pulse generator **130** may apply a first pulse **205B** of the plurality of pulses, which together may form the second waveform **200B**, to the second write state machine **125B**. Thus, in an exemplary embodiment, the initial pulse **205A** of the first waveform **200A** may be applied to the first write state machine **125A** and then the initial pulse **205B** of the second waveform **200B** may

be applied to the second write state machine **125B** at a time of at least 2 microseconds after the initial pulse **205A** of the first waveform **200A**. Therefore, in an exemplary embodiment, the second initial pulse **205B** may occur during the time of the first delay **210** of the first waveform **200**, and thus, in an exemplary embodiment, the second waveform **200B** may be delayed a period equal to Δt. Those skilled in the art will appreciate that the length of the time-delay Δt between the first waveform **200A** and the second waveform **200B** may be in the range of microseconds so that the entire second initial pulse **205B** may occur during the first delay **210** in the waveform **200A** having a plurality of pulses applied to the first write state machine **125A**.

[0025]   FIG. 5 is a timing diagram illustrating a pair of current waveforms **200A**, **200B** for programming a stacked memory array **115** in accordance with another embodiment of the present invention. In an exemplary embodiment, the pulse generator **130** may apply the first pulse **205A** of current of the plurality of pulses, which together may form the first waveform **200A**, to the first write state machine **125A**. Then, the delay circuit **135** may inject a time-delay Δt before the pulse generator **130** may apply a first pulse **205B** of the plurality of pulses, which together may form the second waveform **200B**, to the second write state machine **125B**. Thus, the initial pulse **205A** of the first waveform **200A** may be applied to the first write state machine **125A** and then the initial pulse **205B** of the second waveform **200B** may be applied to the second write state machine **125B** at some time after the initial pulse **205A** of the first waveform **200A**. Therefore, in an exemplary embodiment, the second initial pulse **205B** may occur during the time of the second delay **230** of the first waveform **200**, and thus, in an exemplary embodiment, the second waveform **200B** may be delayed a period equal to Δt. Those skilled in the art will appreciate that the length of time the second waveform **200B** may be delayed may be in the range of 93 microseconds to 111 microseconds so that the entire second initial pulse **205B** may

occur during the second delay **230** in the waveform **200A** having a plurality of pulses applied to the first write state machine **125A.**

[0026] Also, those skilled in the art will appreciate the length of time that the second waveform **200B** may be delayed may be other amounts of time so long as that when the total amount of current in the system **100** is aggregated, the voltage regulator may accommodate the aggregated current. Thus, it may be within the scope of the embodiments of the present invention to delay the second initial pulse **205B** that may be applied to the second write state machine **125B** such that a portion of the second initial pulse **205B** may overlap a portion of the first initial pulse **205A** that may be applied to the first write state machine **125A**. Because in some exemplary embodiments, the peak amplitudes of the two initial pulses **205** may not occur simultaneously, a standard voltage regulator may accommodate the total current of the system **100** at any given time.

[0027] In exemplary embodiments, the time delay Δt between the first waveform **200A** and the second waveform **200B** may be between 2 and 111 microseconds, which may create a minimal delay in the amount of time the system **100** requires to program the memory arrays **120**, as compared to the seconds added if the write state machines **125** were to be programmed sequentially. Additionally, by creating a time-delay Δt between the two waveforms **200** applied to the two write state machines **125**, the overall cost of manufacturing and operating the system **100** may decrease as compared to the cost of manufacturing and operating a system in which the write state machines **125** are programmed in parallel (i.e., simultaneously). This is due in part to the fact that in many cases, a new regulator should be added to the system to accommodate the larger amounts of current and in part to the fact that a lesser amount of current may be applied simultaneously.

[0028]   FIG. 6 is a timing diagram illustrating a pair of current waveforms **600** for programming a stacked memory array **115** in accordance with still another embodiment of the present invention. Waveforms **600** may include a series of pulses **605** therein wherein all pulses **605** may be of equal amplitude, duration, and period. In an exemplary embodiment, the pulse generator **130** may apply the first pulse $605A_1$ of current of the first waveform **600A**, to the first write state machine **125A**. Then, the delay circuit **135** may inject a time-delay Δt before the pulse generator **130** may apply a first pulse **605B** of current of the second waveform **600B** to the second write state machine **125B**. Therefore, in an exemplary embodiment, the second initial pulse **605B** may occur during the time of a first delay $610A_1$ of the first waveform **600A**, and thus, in an exemplary embodiment, the second waveform **600B** may be delayed a period equal to Δt.

[0029]   Other alternative embodiments will become apparent to those skilled in the art to which an exemplary embodiment pertains without departing from its spirit and scope. Accordingly, the scope of the embodiments of the present invention may be defined by the appended claims rather than the foregoing description.